About Electronics & ICT Academy at PDPM IIITDM Jabalpur

The Ministry of Electronics and Information Technology (MeitY), Government of India has instituted Electronics and ICT Academies in the year 2015. In the second phase, the academy at PDPM IIITDM Jabalpur aims at scalable training programmes in niche areas of Electronics and ICT for the development of the required knowledge base, skills and tools to unleash the talent of the Indian population. In addition to the faculty development programmes (FDPs) on fundamental and advanced topics in electronics, information and communication technologies, the Academy conducts customized training programmes for students, corporate sectors and research promotion workshops in emerging areas. The Academy is identified by the MeitY as the central hub of activities on training, internships, research, and consultancy programmes.

About PDPM IIITDM Jabalpur

PDPM IIITDM Jabalpur was established in 2005 with a focus on education and research in IT-enabled Design and Manufacturing. Since its inception, PDPM IIITDM Jabalpur has been playing a vital role in producing quality human resources for contribution to India's mission of inclusive and sustainable growth. The Institute offers undergraduate, postgraduate and PhD programmes in Computer Science and Engineering, Electronics and Communication Engineering, Mechanical Engineering, Design and PhD programmes in Mathematics, Physics and Literature. Further, the Institute offers an undergraduate programme in Smart Manufacturing. Under IIIT act, the Institute has been declared as an Institute of National Importance. The Institute campus is developed on 250 acres of land close to Dumna Airport, Jabalpur. The Institute is 10 kms from the main railway station and 5.5 kms from Dumna Airport, Jabalpur.

Faculty Development Programme

Semiconductor Chip Design

The FDP will provide in-depth knowledge to the participants regarding the recent trends in the field of semiconductor chip design covering topics such as fundamentals of IC Design, simulation and modelling of cutting-edge semiconductor devices low power VLSI Design and fabrication methodologies. Hands-on sessions will equip the participants with the skills and expertise in the field of IC Design and Semiconductor Device Modelling. The FDP is aligned with the Indian Semiconductor Mission (ISM) initiative of the Government of India to develop skilled workforce in the field of Semiconductor Technology.

Who can attend: The Programme is open to faculty from all colleges, universities, and technical and professional institutes. Students, fresh graduates, researchers, and industry personnel working in allied disciplines can also attend.

Important Dates:

Last Date of Online Registration: June 20, 2025

FDP Dates: July 1-11 2025

Coordinators:

Dr. Dip Prakash Samajdar, Department of ECE, PDPM IIITDM Jabalpur

Dr Neeraj Jaiswal, Department of Natural Science, PDPM IIITDM Jabalpur

Contact us:

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Faculty Development Programme

Semiconductor Chip Design

July01-11, 2025 (Online mode)

Electronics and ICT Academy, Phase II

Digital India
Power To Empower

An Initiative of
Ministry of Electronics and Information Technology,
Government of India

PDPM IIITDM JABALPUR

PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur
Dumna Airport Road, Jabalpur 482005

Faculty Development Programme
Semiconductor Chip Design

July 1-11, 2025 (Online Mode)

RESOURCE PERSONS

- Prof. Santosh Vishwakarma, IIT Indore
- Prof. Jawar Singh, IIT Patna
- Dr. Vibhuti Chauhan, MANIT Bhopal
- Dr. Dhramendra Singh, NIT Kurukshetra
- Dr. Chitraja Rajan, RCOEM Nagpur
- Ms. Pooja Kumawat, NVIDIA
- Dr Balwinder Raj, NIT Jalandhar
- Dr Kumar Prasannajit Pradhan, IIITDM Kancheepuram
- Mr Amit Saini, Cadre Systems
- Dr Pankaj Sharma, PDPM IIITDM Jabalpur

COURSE COORDINATORS

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Course Contents

- Basics of VLSI Design
- Logic Design with MOSFETs
- Analysis of CMOS Logic Gates
- High-Speed CMOS Circuits
- System Level Physical Design
- Analog VLSI Design
- Low Power VLSI Design
- CMOS Memories
- IC Fabrication Methodologies
- Machine Learning in VLSI
- VLSI Circuits

Hands-On Sessions

- VLSI Circuit Design using Open Source EDA Tools
- Semiconductor Device Simulation with TCAD

Programme Features

- Fundamentals of Semiconductor Chip design and IC Fabrication
- Opportunities to connect with experts in the field.
- Instructor-led rigorous hands-on sessions.
- Certificate on successful completion with full access to the course material.

Registration Details

- Registration link – Please fill out registration using the following link: https://forms.gle/AqdhU42gEvuzVfgT7

- Registration fee: 500 INR/- (For Online)
- Last Date for Registration: June 20, 2025

Online Payment Details

- **Internet banking**

Beneficiary Name	PDPM IIITDM Jabalpur
Bank Name	INDIAN BANK
A/C No.	50018692852
IFSC Code	IDIB000M694

- **UPI ID: iiitdmj@indianbk**